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EXAMINER	
NGUYEN, LUONG TRUNG	
ART UNIT	**PAPER NUMBER**
2622	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,442	NAKAMURA, KENJI	
	Examiner	Art Unit	
	LUONG T. NGUYEN	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-3, 8-11 filed 3 /13/2006 have been fully considered but they are not persuasive.

Applicant's arguments, see Amendment, filed on 3/13/2006, with respect to claims 4-7 have been fully considered and are persuasive. The rejection under 35 U.S.C. 103(a) as being unpatentable over Tomaszewski in view of Clemens further in view of Suzuki et al. and Anderson et al. of claims 4-7 has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Clemens , Jolley et al., Anderson et al. and Theron et al.

In re page 7, Applicant argues that Suzuki does not disclose that the PLD, etc. is reconfigured to provide different logic circuits so as to selectively provide a camera with a plurality of functions according to a camera operation selected by the user. Indeed, Suzuki provides no suggestion or teaching with respect to employing a reconfigurable circuit in this manner.

In response, the Examiner disagrees. The Examiner considers that Suzuki et al does disclose a reconfigurable circuit. Suzuki et al. discloses a CPU 34 is preferably implemented on special purpose computer, a programmed microprocessor, an ASIC or other integrated circuit elements, a hardwired electronic or logic circuit such as a discrete element circuit, a programmable logic device such as a PLD, PLA, FPGA or PAL (Note that Field Programmable

Gate Array (FPGA) includes a large number of configurable logic blocks, which can be considers as a re-configurable circuit and can be reconfigured in a selected mode, section [0054], page 3). In addition, it is noted that the Applicant considers the re-configurable circuit is a field programmable gate array as recited in claim 3.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 8, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. 2002/0057351) in view of Suzuki (U. S. Patent No. 6,380,975).

Regarding claim 1, Suzuki et al. discloses a camera comprising a user operable member for accepting a user operation (touch tablet 6A, Figure 12, Page 7, Sections [0106]-[0113]); a mode selector (Figure 12 shows that the user can select mode, such as recording mode, playback mode) for selecting one of a first mode (recording mode, Figure 12, Page 7, Section [0112]) for executing first image data processing (processing image data by DSP 33, compression/expansion circuit 38, buffer memory 37, memory card 24, Figure 4, Page 7, Section [0112]) to an image data taken by an image pickup device (CCD 20, Figure 4) and a second mode (playback mode, Figure 12, Page 7, Section [0112]) for executing second image data processing contents of which are different from that of the first image data processing (image data recorded in memory card is read out through buffer memory, compression/expansion circuit

38, LCD 6, Figure 4, Page 7, Sections [0056], [0112]); a re-configurable circuit in which a logic circuit is obtained by a predetermined program, said logic circuit is configured depending on the program, and said logic circuit executes a predetermined operation on inputted image data (programmable logic device such as PLD, PLA, FGPA, PAL. Note that Field Programmable Gate Array (FPGA) includes a large number of configurable logic blocks, which can be considers as a re-configurable circuit and can be reconfigured in a selected mode, section [0054], Page 3).

Suzuki et al. fails to specifically discloses a memory for memorizing a first program corresponding to the first image data processing and a second program corresponding to the second image data processing; and a controller for reading the first program from the memory and re-configuring the re-configurable circuit based on the first program so as to configure a first logic circuit when the first mode is selected by the mode selector and for reading the second program from the memory and re-configuring the re-configurable circuit based on the second program so as to configure a second logic circuit when the second mode is selected by the mode selector. However, Suzuki et al. discloses CPU 34 is a programmed microprocessor controls processing image data readout from CCD 20 to be recorded on memory card 24 or to be displayed on LCD 6, Page 3, Section [0054]. And Suzuki ('975) discloses a digital camera, in which an image compressing/extending means is realized by a control program stored in the CPU 113 (Column 30, Lines 21-36). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Suzuki et al. by the teaching of Suzuki ('975) in order to execute compression or expansion by program. This

improves operability and convenience in data transfer from a digital camera to an external device (Column 30, Lines 12-14).

Regarding claim 2, Suzuki et al. discloses the first mode is an image pickup mode for taking an image data by photoelectric transferring an optical image of an object (recording mode, CCD 20 electrically converts the light image into image signals; the image signals are recorded on memory card 24 via compression circuit 38, Figures 4, 12, Page 7, Section [0112]); the second mode is a reproducing mode (playback mode, Figures 4, 12, Page 7, Section [0112]) for reproducing an image on a display (LCD 6, Figure 4, Page 3, Section [0056]) by using an image data taken by the image pickup mode; the first image data processing is a data compression processing of the image data taken by the image pickup mode (compression in compression/expansion circuit 38, Figure 4, Page 3, Section [0051]); and the second image data processing is a data extension processing of a compressed image data (expansion in compression/expansion circuit 38, Figure 4, Page 3, Section [0056]).

Regarding claim 3, Suzuki et al. discloses the re-configurable circuit is a field programmable gate array FGPA, Page 3, Section [0054]).

Regarding claim 8, Suzuki et al. discloses a camera comprising a user operable member for accepting a user operation (touch tablet 6A, Figure 12, Page 7, Sections [0106]-[0113]); an image processing selector for selecting an image processing among a plurality of image processing corresponding to different characteristics with respect to quality of an image, wherein

said image processing selector selects the image processing in accordance with the user operation accepted via the user operable member (Figure 12 shows that the user can select mode, such as image processing for recording mode or playback mode); a re-configurable circuit in which a logic circuit is obtained by a predetermined program, said logic circuit is configured depending on the program, and said logic circuit executes a predetermined operation on inputted image data input to the re-configurable circuit (programmable logic device such as PLD, PLA, FPGA, PAL. Note that Field Programmable Gate Array (FPGA) includes a large number of configurable logic blocks, which can be considers as a re-configurable circuit and can be reconfigured in a selected mode, section [0054], Page 3).

Suzuki et al. fails to specifically disclose a memory for memorizing a plurality of programs corresponding to the plurality of image processing; and a controller for reading a program corresponding to the image processing selected by the image processing selector and re-configurable circuit so as to configure a first logic circuit based on one among the plurality of programs or a second logic which is different from the first logic circuit based on another one among the plurality of program. However, Suzuki et al. discloses CPU 34 is a programmed microprocessor controls processing image data readout from CCD 20 to be recorded on memory card 24 or to be displayed on LCD 6, Page 3, Section [0054]. And Suzuki ('975) discloses a digital camera, in which an image compressing/extending means is realized by a control program stored in the CPU 113 (Column 30, Lines 21-36). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Suzuki et al. by the teaching of Suzuki ('975) in order to execute compression or expansion by program.

This improves operability and convenience in data transfer from a digital camera to an external device (Column 30, Lines 12-14).

Regarding claim 11, Suzuki et al. discloses the re-configurable circuit is a field programmable gate array FPGA, Page 3, Section [0054]).

4. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clemens (WO 99/40723) in view of Jolley et al. (U. S. 6,073,201) further in view of Anderson et al. (U. S. Patent No. 6,567,122) and Theron et al. (U. S. 6,631,520).

Regarding claim 4, Clemens discloses a camera (Camera 10, Figure 1) comprising a connection portion (a connector connects to cable 14, Figure 1, Page 5) to which a first equipment (USB, Page 8) and a second equipment (RS-232 serial interface, Page 8) can be alternatively be connected, the first equipment being communicative with the camera by a first data communication standard (the digital camera 10 is tethered to the computer 12 by the cable 14, which can be Universal Serial Bus (USB), Figure 1, Page 8), and the second equipment being communicative with the camera by a second data communication standard different from the first data communication standard (the digital camera 10 is tethered to the computer 12 by the cable 14, which can be RS-232 serial interface, Figure 1, Page 8).

Clemens fails to specifically disclose a detector for judging a kind of data communication standard of an equipment connected to the connection portion. However, Jolley et al. teaches a multiple interface input/output port for a peripheral device that is capable of automatically detecting the type of interface bus to which it is connected in a host computer and then routing

communications between the two device through an appropriate interface adapter (Figure 1, Column 2, Lines 44-67, Column 4, Lines 40-63). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Clemens by the teaching of Jolley et al. in order to connect a digital camera to a computer by a multiple interface input/output port for a peripheral device that is capable of automatically detecting the type of interface bus to which it is connected in a host computer and then routing communications between the two device through an appropriate interface adapter (Column 2, Lines 32-37).

Clemens and Jolley et al. fail to specifically disclose a memory for memorizing a first program corresponding to a first image data communication processing fitting for the first data communication standard and a second program corresponding to a second image data communication processing fitting for the second data communication standard. However, Anderson et al. discloses a digital camera, in which an application software for operating USB bus or IEEE 1394 bus is stored in DRAM 346, Figures 3, 9, Column 12, Lines 23-40). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Clemens and Jolley et al. by the teaching of Anderson et al. in order to store program for controlling connection between a digital camera and a computer.

Clemens, Jolley et al. and Anderson et al. fail to specifically disclose a re-configuration circuit in which a logic circuit is obtained by a predetermined program, said logic circuit is configured depending on the program, and said logic circuit executes a predetermined operation on inputted image data; a controller for reading the first program from the memory and re-configuring the re-configuration circuit based on the first program so as to configure a first logic

circuit when the kind of the data communication standard of the equipment connected to the communication portion is judged as the first data communication standard by the detector and for reading a second program from the memory and re-configuring the re-configuration circuit based on the second program so as to configure a second logic circuit when the kind of the data communication standard of the equipment is judged as the second data communication standard. However, Theron et al. discloses an apparatus for changing execution code for a microcontroller on an FPGA interface device, which comprises an interface 30, the interface 30 includes an on-board FPGA 32, a microcontroller 34, Universal Serial Bus (USB) interface 40 and a RS-232 serial port interface 42, which are coupled to the USB and serial ports, respectively (Note that Field Programmable Gate Array (FPGA) includes a large number of configurable logic blocks, which may be configured in either a serial mode or a parallel mode, Figure 3, Column 4, Lines 23-45; Column 5, Line 15 – Column 6, Line 20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Clemens, Jolley et al. and Anderson et al. by the teaching of Theron et al. in order to provide to a device an on-board FPGA, which allows for simultaneous storage of both a default on-board FPGA configuration and a new on-board FPGA configuration and allows on-board FPGA to reconfigure itself at any time using either configuration (Column 8, Lines 42-45).

Regarding claim 5, Clemens discloses the first data communication standard and the second data communication standard are respectively a USB standard and an RS-232C standard (Page 8).

Regarding claim 6, Clemens discloses wherein the equipment to be connected to the connection portion is an equipment which can execute an image data processing (the captured image is transferred to computer 12 via cable 14, Figure 1, Page 5).

Regarding claim 7, Theron et al. discloses the electronic circuit arrangement is a field programmable gate array (PGPA, Figure 3, Column 4, Lines 23-30; Column 7, Lines 40-45).

5. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U. S. 2002/0057351) in view of Suzuki (U. S. Patent No. 6,380,975) further in view of Nakamura (U. S. Patent No. 6,278,492).

Regarding claim 9, Suzuki et al. and Suzuki ('975) fail to specifically disclose the image processing with respect to the quality of the image is a gamma compensation. However, Suzuki et al. discloses the digital signal processor DSP 33 processes image data and supplies image data to memory card 24 via buffer memory 37, Figure 4, Page 3, Section [0051]. And Nakamura discloses a camera, in which image signal output from A/D conversion circuits 15R, 15G and 15B are sent to digital processing circuit 16, which processes the image signals with digital signal processing such as gamma processing (Column 4, Line 65 – Column 5, Line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Suzuki et al. and Suzuki ('975) by the teaching of Nakamura in order to improve the quality of the image data.

Regarding claim 10, Suzuki et al. and Suzuki ('975) fail to specifically disclose the image processing with respect to the quality of the image is a contour emphasizing or unemphasizing compensation of the image. However, Suzuki et al. discloses the digital signal processor DSP 33 processes image data and supplies image data to memory card 24 via buffer memory 37, Figure 4, Page 3, Section [0051]. And Nakamura discloses a camera, in which image signal output from A/D conversion circuits 15R, 15G and 15B are sent to digital processing circuit 16, which processes the image signals with digital signal processing such as contour enhancement (Column 4, Line 65 – Column 5, Line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Suzuki et al. and Suzuki ('975) by the teaching of Nakamura in order to improve the sharpness of the image data.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN
06/11/06

LUONG T. NGUYEN
PATENT EXAMINER